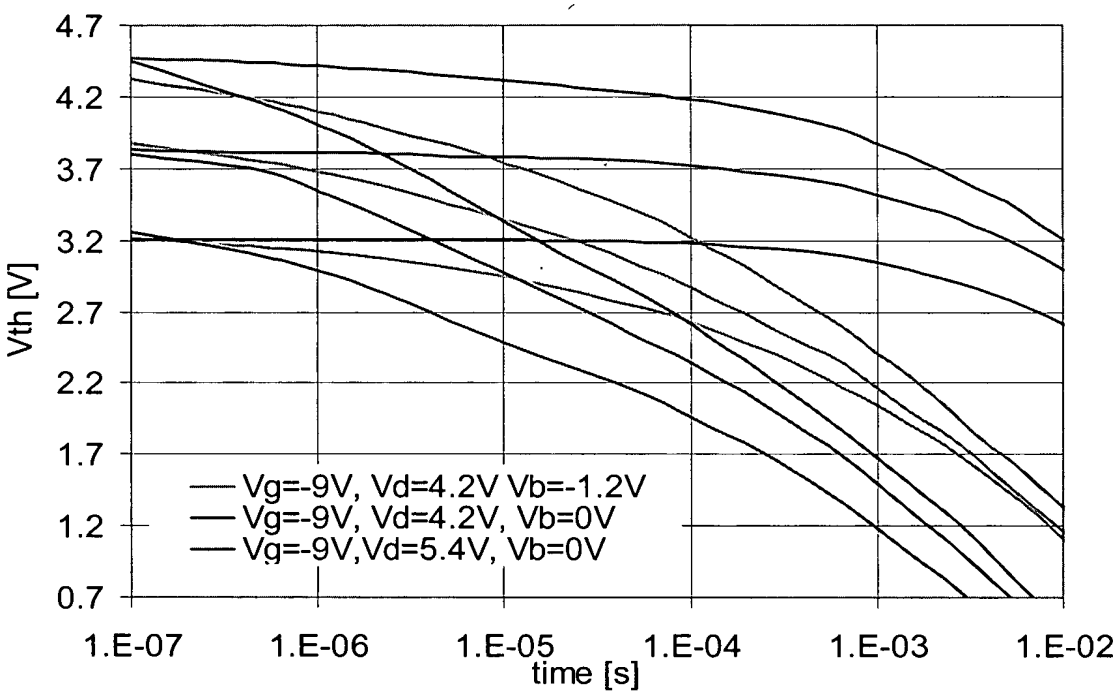

4.7
4.2
3.7
3.2
2.7
2.2
1.7
1.2
0.7
Vth [V]
Vg=-9V, Vd=4.2V Vb=-1.2V
Vg=-9V, Vd=4.2V, Vb=0V
Vg=-9V,Vd=5.4V, Vb=0V
1.E-07
1.E-06
1.E-05
1.E-04
1.E-03
1.E-02
time [s]

FIG. 1

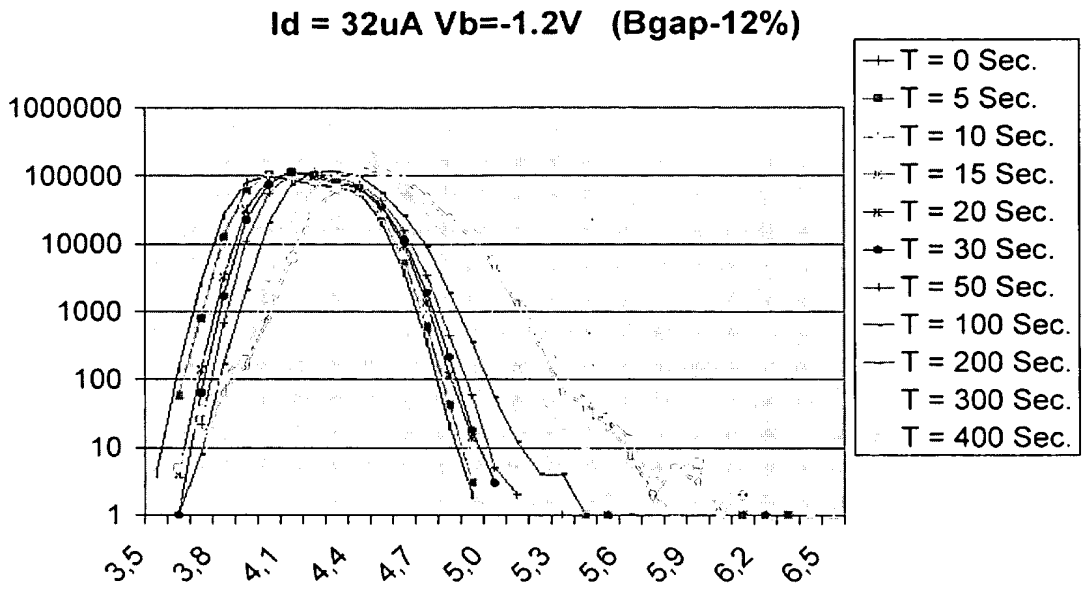
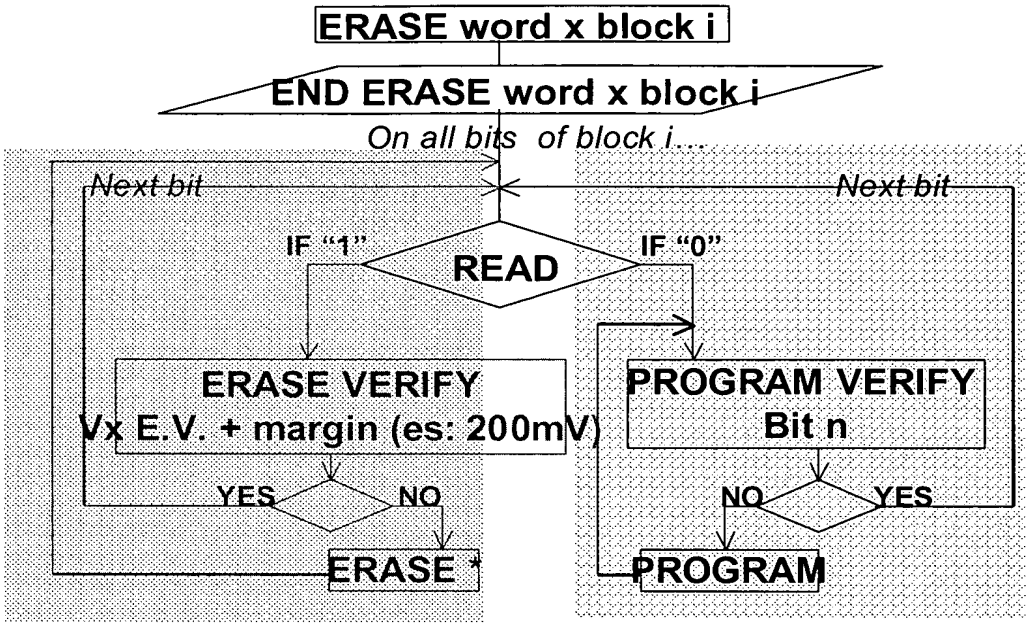

Id = 32uA Vb=-1.2V (Bgap-12%)
1000000
100000
10000
1000
100
10
1
3,5
3,8
4,1
4,4
4,7
5,0
5,3
5,6
5,9
6,2
6,5
T = 0 Sec.
T = 5 Sec.
T = 10 Sec.
T = 15 Sec.
T = 20 Sec.
T = 30 Sec.
T = 50 Sec.
T = 100 Sec.
T = 200 Sec.
T = 300 Sec.
T = 400 Sec.

FIG. 2



During this cycle the critical "1" bit are identified and erased down to erase verify

During this cycle the critical bit "0" are identified and programmed up to program verify

FIG. 3

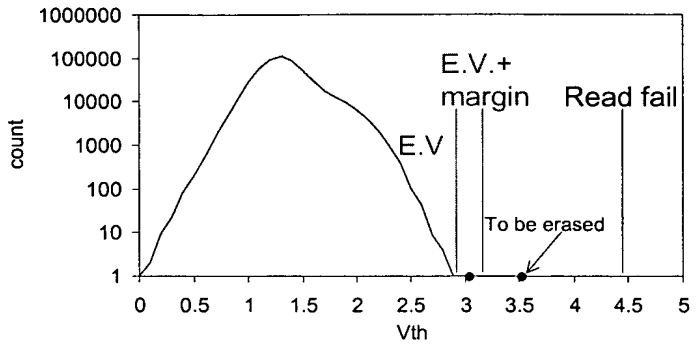

1000000
100000
10000
1000
100
10
1
count
E.V.+
margin
Read fail
E.V
To be erased
0
0.5
1
1.5
2
2.5
3
3.5
4
4.5
5
Vth

FIG. 4